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Application Note **MSAN-144**

Applications of the MT8841 Calling Number Identification Circuit

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Introduction

The purpose of this Application Note is to provide information on the operation and application of calling number identification circuits. The MT8841 Calling Number Identification Circuit (CNIC) will be discussed in detail and its use illustrated in the application examples which follow.

Everyone, at some time, has rushed to answer a ringing phone only to have the caller hang up. We have all had a persistent salesman (or a talkative friend) call our office or home and interrupt us at the wrong time. Many of us have had to sit and listen to elevator music while someone on the other end of the line attempts to bring up information about our account. By allowing call screening and quick access to databases before the phone is answered, Caller ID (CID) promises a cure for many of the annoying telephone problems that beset us.

In a caller ID system, a coded version of the calling number is sent from the central office to the called phone where it appears on a small liquid crystal display (LCD). For both residential and office phones, the subscriber will know who is calling (provided it is a known number) and be able to screen the calls. In more sophisticated applications, when the line is connected to a computer, the computer can use the number to search a database and display information about the individual calling.

Applications

Caller ID technology has many commercial applications. For example, an insurance company could display all the relevant information about a client's policies even before the phone is answered, which would save time for both the company and the customer. A hospital might use this capability to bring up a patient's medical records when they call in. A mail order company could display the buying record of a customer and be ready to conduct business by the time the first word is spoken.

There are many CID implementations. The chip can be used in a small stand-alone unit (with an LCD) connected to the line, or it can be built into a telephone set. It can be used in a computer or on a trunk card in a PBX. There is a growing interest in CID from the companies that are designing the next generation of answering machines.

The answering machine companies want to be able to identify and record the number of callers who hung up without leaving a message. In addition, answering machine users want to be able to program certain numbers that the user doesn't want to talk to so that these calls can be sent directly to the answering machine for recording and later reply. CID technology will also be incorporated in FAX machines and combination FAX/answering machines to allow users to screen for junk Faxes.

Telephone companies view Caller ID as another service to generate revenue. Consequently, the Bell Operating Companies asked Bell Communications Research (Bellcore) to prepare specifications that show manufacturers how to build CID equipment. These describe features and functions of equipment or interfaces for possible use by any divested Bell Operating Company or its regional affiliate. In the Calling Number Delivery (CND) service, the information about a calling party is embedded in the silent interval between the first and second ring. Besides CND, there are other telephone company services that use the same transmission scheme. For example, another service extends CND with call waiting so that customers can tell who is calling on the other line. This requires some handshaking between the phone and the central office. Future devices will incorporate this feature. Calling Name Delivery (CNAM), another service using the same scheme, displays the name of the caller, rather than the number.

How it Works

The principle of CID is relatively simple. Coded signalling information is sent during the period between the first and second ring. Continuous phase binary frequency shift keying (FSK) is used for coding. The CID chip decodes analog information and transforms it into a digital bit stream which is available at the DATA pin. A micro-controller extracts caller information from the digital stream.

A CID system has five important functions: line termination during data reception, high voltage isolation, common mode rejection, ring detection and CID data reception. These functions, with the exception of CID reception, are not built into most CID devices, so a small amount of external circuitry is required.

The receive data dynamic range of the CID detection circuit is a critical requirement. On a long loop the signal strength may be very low, but the CID device must be able to detect it. Consequently, analog performance as shown by the detect level and the ability to perform in the presence of noise is very important. The Mitel Calling Number Identification Circuit (CNIC) for example, has a detect level of -36dBm, specified over the entire temperature range. The device is also specified to operate at a typical 20dB S/N ratio. In addition, the MT8841 has a user accessible input op-amp which can be configured in a differential mode to reduce the effects of common mode noise. The input gain may also be changed easily (either increased or decreased) to meet specific regulatory decode level requirements. This is accomplished by changing the resistor values of the input op-amp network.

According to the Bellcore specifications, the Customer Premises Equipment (CPE) should terminate the transmission line with the correct impedance while data is being transmitted. The CPE must detect the end of the first power ring and switch in the termination. The termination is external to the CID chip and is typically connected with a relay during the period between the first and second ring signals.

For applications requiring reduced power consumption, a power down mode is desirable. The MT8841 has a power down pin (PWDN), which when pulled high, forces the device into power down. This is typically done after receiving a message. In this mode, the CID device ceases to function and the chip will not react to an input signal. Pulling the pin to ground wakes up the chip so that it can receive the FSK signal and start decoding.

A Three-Pin Interface

Most CID devices only provide a single pin from which the received data is sent to the micro-controller. Consequently, the data stream appearing at the serial data output must be converted to 8-bit words by a UART (Universal Asynchronous Receiver Transmitter). The Mitel CNIC, however, has three pins dedicated to the user interface. This eliminates the need for a UART or the high software overhead of a micro-controller performing the UART function (asynchronous serial data reception). Refer to the MT8841 data sheet and Figure 1 below.

General Requirements for Calling Number Delivery Service

According to the Bellcore Technical Reference TR-NWT-000030, the Central Office physical layer interface has the following parameters for providing CND service:

Link Type:	two wire, half-duplex from SPCS to CPE
Modulation Type:	Continuous-phase binary FSK
Logical 1 (Mark):	1200 ±12 Hz
Logical 0 (Space):	2200 ± 22 Hz
Transmission Rate:	1200 ±12 baud
Signal Level:	-13.5 dBm ± 1.5dB at the point of application to the loop facility into a resistive load of 900 ohms.
Source Impedance:	900 ohms in series with 2.16 µF to meet return loss requirements specified in TR-TSY-000507.
Application of Data:	Serial, binary, asynchronous

To properly interact with SPCS for both on-hook and off-hook data transmission schemes, the CPE should receive a data signal that meets the following parameters:

- Link Type, Modulation Type, Transmission Rate, Application of Data, Logical 1 (Mark) and Logical 0 (Space): same as Central Office transmit values shown above.
- Received Signal Level at 1200 Hz: between -32 dBm and -12.5 dBm.
- Received Signal Level at 2200 Hz: between -36 dBm and -12.5 dBm.
- Signal to Distortion Ratio: > 25 dB.

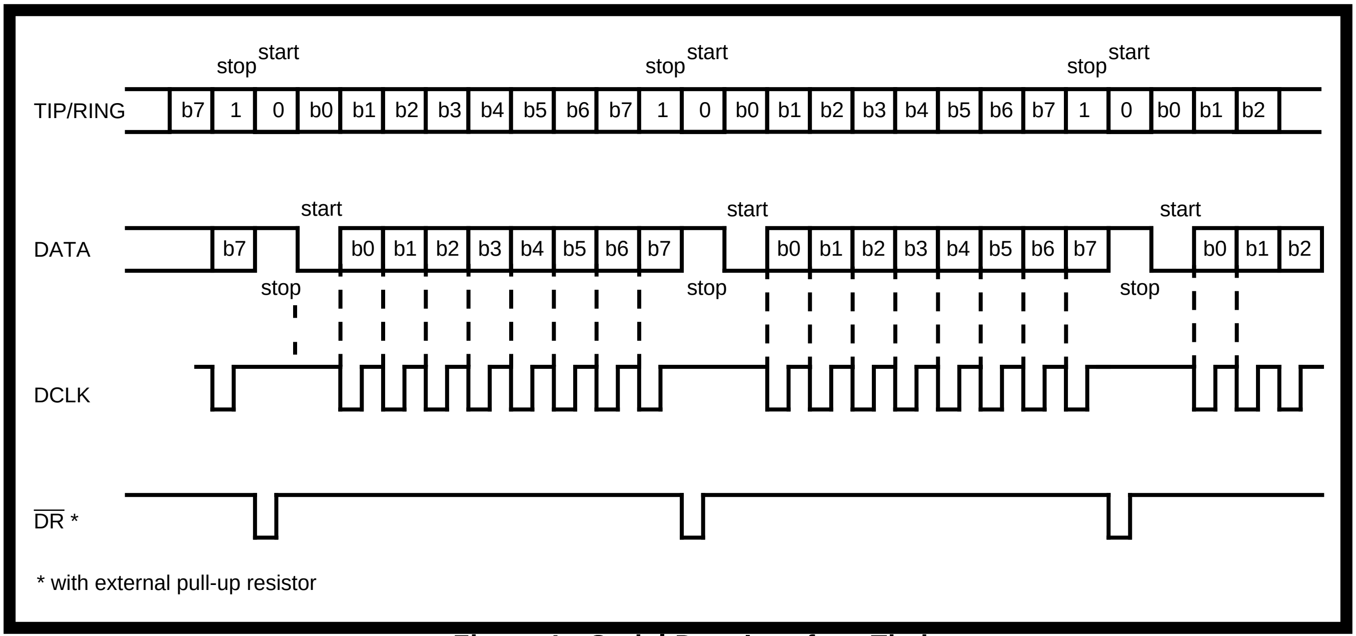


Figure 1 - Serial Data Interface Timing

Data Transmission Methods and Message Formats

The CNIC can process a FSK modulated signal carrying information compatible with any of the three data transmission methods specified by TR-NWT-000030:

- On-hook data transmission associated with ringing,
- On-hook data transmission not associated with ringing,
- Off-hook data transmission.

The SPCS data interface supports single data message and multiple data message formats. In the single data message format, information is sent to the CPE as a series of data words specifying message type, message length, message data and error detection information. In the multiple data message format, information sent to the CPE is similar to the single message format except the message data field is replaced by a series of parameter messages. Each parameter message consists of data words specifying parameter type, parameter length and parameter data.

For single and multiple data message formats each word shall consist of an 8-bit data byte preceded by a start bit (space) and followed by a stop bit (mark). The least significant bit of each data byte shall be transmitted first. The Mark bits (maximum ten bits of high) may also be inserted between message words when necessary. Since the FSK modulation is used in both data message formats, the differences between the two formats are transparent to the CNIC.

Briefly, the CND multiple data message format consists of the following:

channel seizure signal (1)	mark signal (2)	message type word (3)	message length word (4)	parameter messages (5)	check sum word (6)

Field (1): The channel seizure signal, used for on-hook data transmission only, is a block of 300 continuous bits of alternating "0"s and "1"s. The first bit to be transmitted is "0" while the last bit is "1".

Field (2): The Mark signal is composed of 80 ±10 bits of continuous high.

Field (3): 1 byte of Message type word.

Field (4): The Message length is the 1-byte information that specifies the total number of message data words (for single data message format) or parameter words (multiple data message format) sent to the CPE, excluding the final checksum.

Field (5): Parameter messages can consist of N parameters and each parameter is further divided into three sub-fields in the order shown below:

Parameter Type Word (1 byte)

Specifies the interpretation of the sub-field Parameter Data Words. Possible message types include: time, dialable directory number (DDN), absence of DDN and call qualifier.

Parameter Length Word (1 byte)

Equals the number of data bytes contained in the Parameter Data Words sub-field.

Parameter Data Words

Possible data words include: date, time, incoming call number and reason for absence of DDN. Note all data bytes in this sub-field are encoded in ASCII format.

Field (6): 1 byte binary checksum = 2's complement of {field (3) + field (4) + field (5)} mod 256.

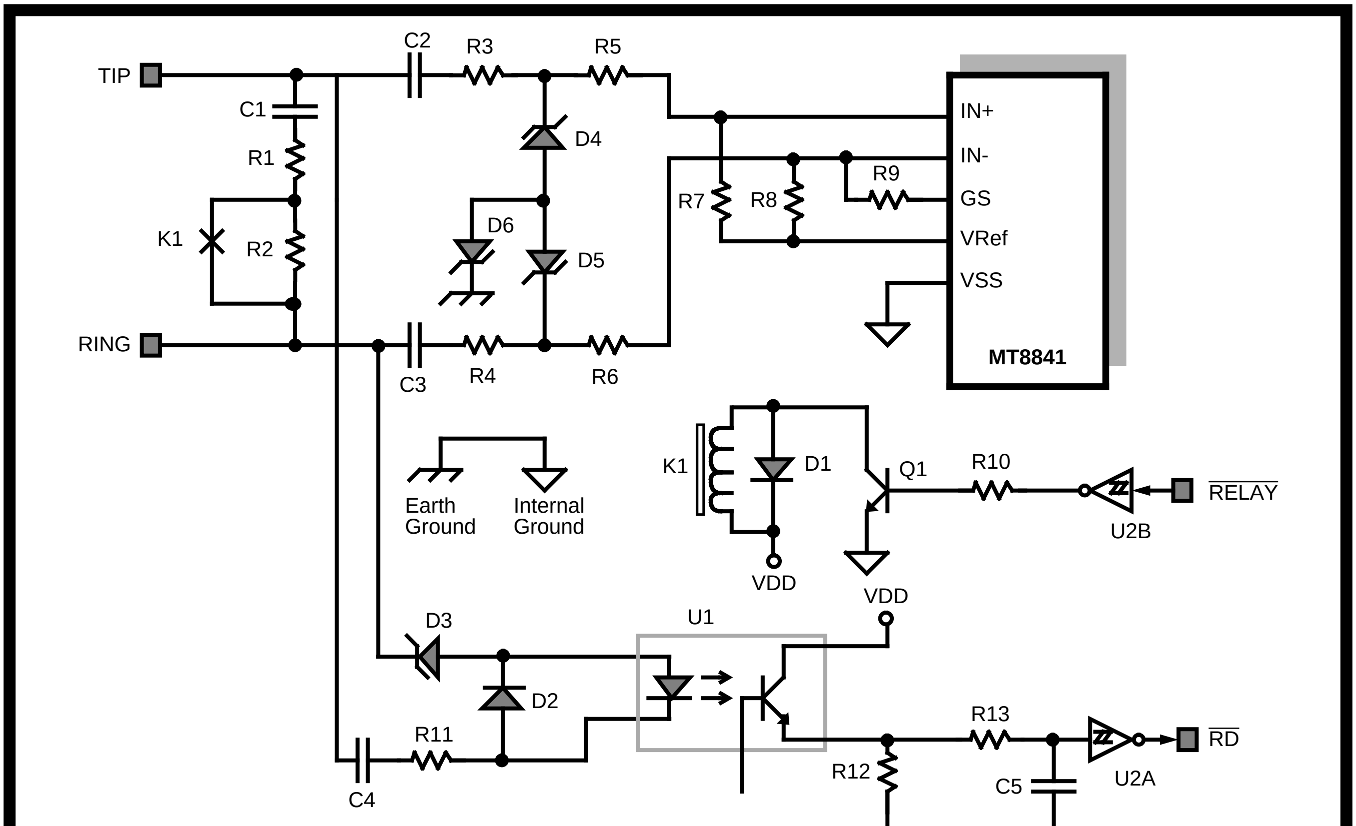
mk: mark bits (0-10)

Application Circuits Using the MT8841

Five Function Telephone Line Interface

The telephone line interface in Figure 2 performs five basic functions, mentioned previously. It terminates the line with 600 ohms, provides high voltage isolation, provides common mode rejection with a differential input, detects ringing, and converts the calling number FSK signal to a serial data format.

During FSK signal reception, the line must be terminated with 600 ohms AC coupled. A termination circuit with relay and relay driver is typically used for



Components List:

U1	4N25, Opto-Coupler	R5, R6	34K, 1/2W 1%, Resistor Metal
U2	74HC14, Inverter Schitt Hex	R7	53k6, 1/2W 1%, Resistor Metal
D2, D1	IN4004, 400V 1A, Rectifier General	R8	60k4, 1/2W 1%, Resistor Metal
D3, D4, D5, D6	IN5245B, 15V 1/2W, Zener General	R13	140k, 1/2W 1%, Resistor Metal
Q1	2N3904, 40V 200mA, Transistor NPN	R12	301k, 1/2W 1%, Resistor Metal
C2, C3	0.022µ, 400V 5%, Capacitor Polyester	R9	464k, 1/2W 1%, Resistor Metal
C5	0.33µ, 50V 20%, Capacitor Ceramic	R1	600r, 1/2W 5%, Resistor Fusible
C4	0.33µ, 250V 5%, Capacitor Polyester	R11	12k, 1W5 5%, Resistor Fusible
C1	2µ2, 250V 5%, Capacitor Polyester	R2, R3, R4	430k, 3W 5%, Resistor Power 1KV
R10	1k, 1/2W 1%, Resistor Metal	K1	RDPDT, 5V 28mA, Relay DPDT

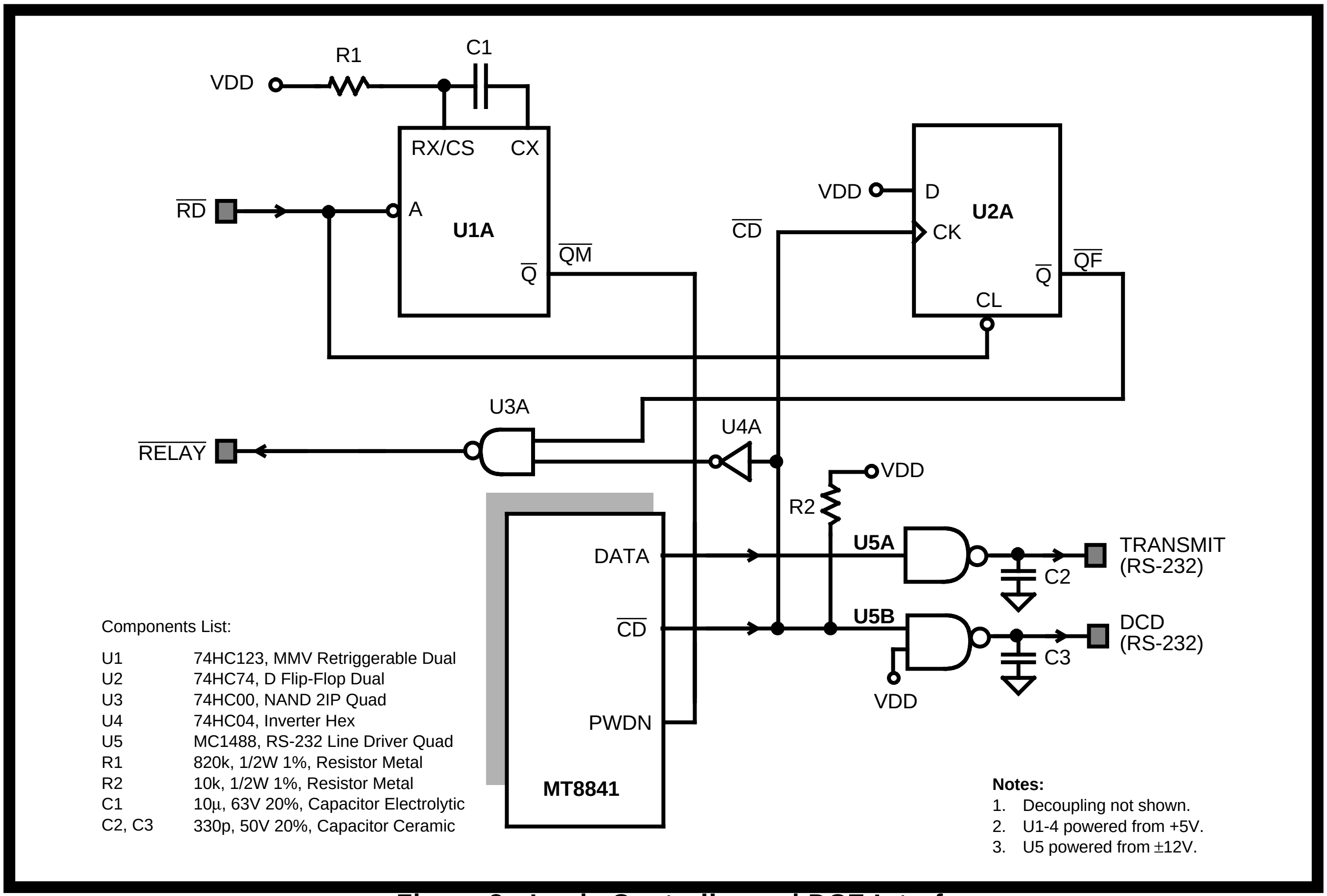
Figure 2 - Line Interface with Protection, Termination and Ring Detector

this function as shown in Fig. 2. When relay K1 is activated (during data reception), the telephone line is terminated with 600Ω (R1) and 2.2µF (C1). A 430k resistor (R2) ensures that capacitor C1 is biased with the 48V CO (central office) battery voltage when relay K1 is not activated. This reduces undesirable transients when the termination circuit is activated.

The high impedance isolation circuit protects the user and the low voltage circuitry from high voltage fault conditions which may occur on the line. The high power resistors and high voltage capacitors (C2, C3, R3, R4), were selected to meet most line fault conditions. The high impedance components limit the current, while the zener's (D4, D5, D6) limit the voltage. Relay K1 and opto-coupler U1 also provide physical isolation.

In the ringing detector of Figure 2, the ringing response is determined mainly by the charge time of C5 through R13, as well as the positive going threshold of the CMOS Schmitt trigger. The ringing detector decay time is determined mainly by the discharge time of C5 through R12 and R13, as well as the negative going threshold of the CMOS Schmitt trigger. Typical response time is 150ms and typical decay time is also 150ms.

The FSK signal data is input to the MT8841 through a differential amplifier configuration with overall gain of unity. To increase the common mode rejection range, a modified differential input configuration is used. A voltage divider of R7 (53.6k) and R3 + R5 (464k) reduces the op-amp signal at the positive input by 9.66 times. To maintain an overall gain of 1, the attenuation due to the voltage divider must be cancelled. This is achieved by increasing the op-amp gain to 9.66. Therefore, 9.66 = 1 + R9/(R8//(R4+R6)); with R9 at 464k, R8 is 60.4k. Since the op-amp common mode range is 3Vpp, the maximum common mode input signal that this circuit can cancel is 3Vpp ° 9.66 = 29Vpp = 10.2Vrms.



Components List:

U1	74HC123, MMV Retriggerable Dual
U2	74HC74, D Flip-Flop Dual
U3	74HC00, NAND 2IP Quad
U4	74HC04, Inverter Hex
U5	MC1488, RS-232 Line Driver Quad
R1	820k, 1/2W 1%, Resistor Metal
R2	10k, 1/2W 1%, Resistor Metal
C1	10µ, 63V 20%, Capacitor Electrolytic
C2, C3	330p, 50V 20%, Capacitor Ceramic

Notes:

1. Decoupling not shown.
2. U1-4 powered from +5V.
3. U5 powered from ±12V.

Figure 3 - Logic Controller and DCE Interface

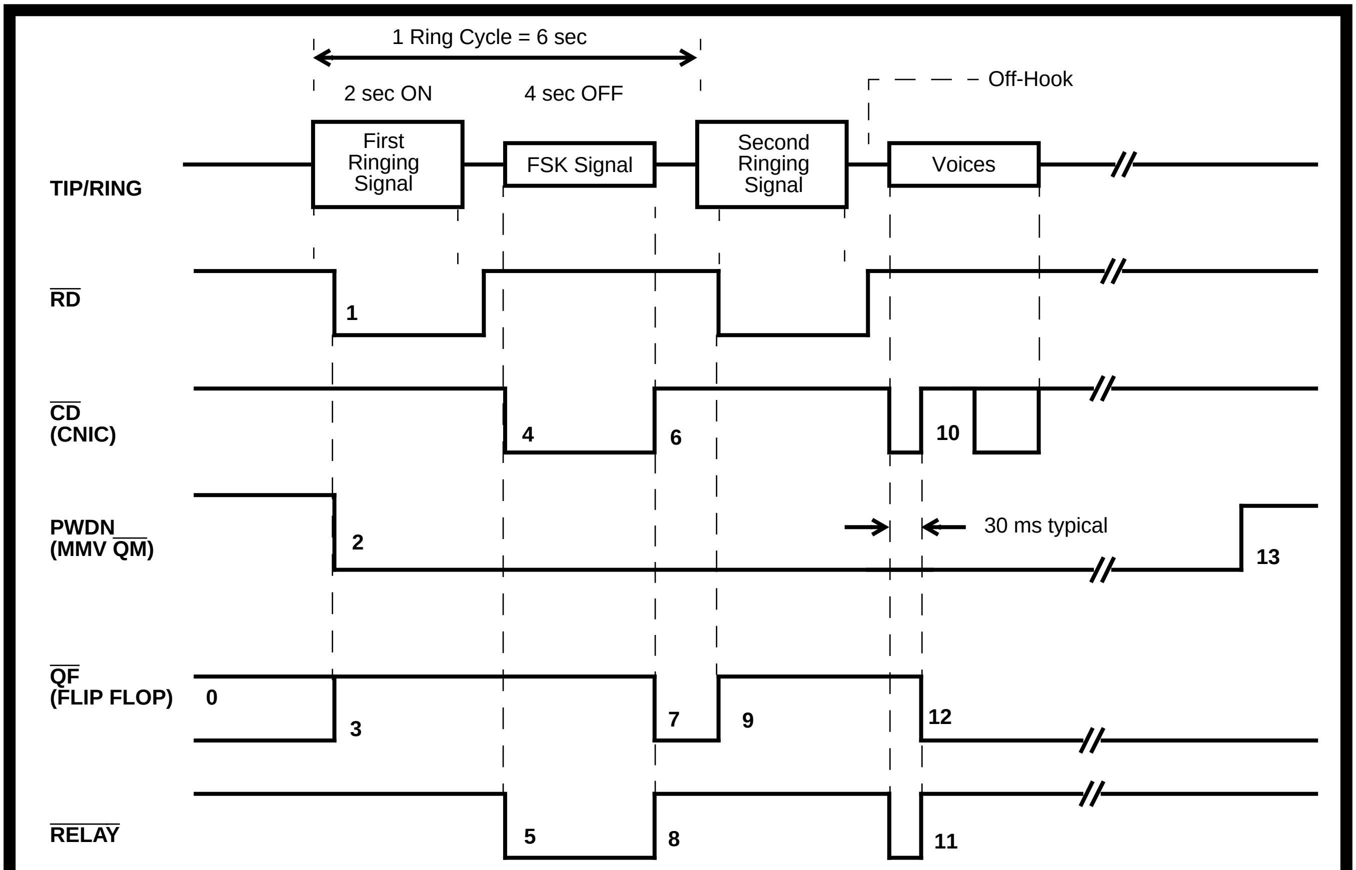
Normally, the device is powered down, but during FSK signal reception, it is powered up. A discrete logic solution is shown in Fig. 3 which provides the relay termination ($\overline{\mathrm{RELAY}}$) and the MT8841 powerdown (PWDN) control signals during the period between the first and second ringing bursts. The above two logic signals are generated by four integrated circuits (U1 to U4). Input signals to the controller are from the ringing detector ($\overline{\mathrm{RD}}$), and CNIC carrier detect ($\overline{\mathrm{CD}}$) outputs. The timing diagram for the logic controller is shown in Fig. 4. Since the relay termination is activated by the first carrier detection following the ringing signal, the circuit will also function correctly for distinctive ringing, where two quick ringing bursts are followed by the FSK.

The start of a ringing burst is signalled by the falling edge of the ring detector ($\overline{\mathrm{RD}}$) output. This triggers the Monostable Multivibrator (MMV) which generates an 8 second output pulse at $\overline{\mathrm{QM}}$ that powers up the CNIC. Shortly after the first ringing burst, the central office (CO) sends the FSK signal. The CNIC detects this and the carrier detect output ($\overline{\mathrm{CD}}$) goes low, this activates the termination relay. The end of FSK transmission is signalled with $\overline{\mathrm{CD}}$ going to logic high. This clocks the flip flop resulting in a logic low at the $\overline{\mathrm{QF}}$ output. This deactivates the termination relay which cannot be re-activated until ringing is once again detected followed by a carrier detect signal.

In the RS-232 DCE line driver (Fig. 3), serial data (DATA) and the carrier detect signal ($\overline{\mathrm{CD}}$) from the MT8841 are converted to RS-232 levels and provided as outputs (TRANSMIT and DCD). These may be directly connected to a DCE such as a personal computer with appropriate software.

Micro-Controller Parallel Read

The CNIC micro-controller interface (Fig. 5) is a symbolic circuit showing a micro-controller performing both the logic functions of Fig. 3 and the data handling. The CNIC provides serial data (DATA), data clock (DCLK), and data ready ($\overline{\mathrm{DR}}$) signals that can be used to easily convert data from a serial stream to a parallel stream (see Fig. 1). Conversion is accomplished by connecting the serial data and clock lines to an external shift register like a 74HC164. When the data ready line alerts the micro-controller with an interrupt, it reads the shift register's 8-bit parallel output. Only the 8-bit character information of the 10-bit word is converted, since the DCLK remains high for both stop and start bits. The data ready signal indicates the reception of every 10-bit word sent from the Central Office.



Notes: the objective is to apply the termination impedance between the first and second ringing bursts; during the FSK signal.

0 FLIP FLOP is in unknown state.
1 Ringing is detected, $\overline{RD}$ goes Low.
2 MMV is triggered, CNIC is powered up.
3 FLIP FLOP is reset by $\overline{RD}$ at Low.
4 Carrier is detected, $\overline{CD}$ goes Low.
5 $\overline{RELAY}$ goes Low due to $\overline{QF}$ High and $\overline{CD}$ Low.
6 Carrier is ended, $\overline{CD}$ goes High.
7 FLIP FLOP is clocked by $\overline{CD}$ going High, $\overline{QF}$ goes Low.
8 $\overline{RELAY}$ goes High due to $\overline{QF}$ Low or $\overline{CD}$ High.
9 FLIP FLOP is reset, $\overline{QF}$ goes High.
10 Voice is detected, $\overline{CD}$ toggles between Low and High.
11 $\overline{RELAY}$ momentarily goes Low due to $\overline{QF}$ High and $\overline{CD}$ Low.
12 FLIP FLOP is clocked by $\overline{CD}$ going High, $\overline{QF}$ goes Low and remains Low until ringing is detected.
13 MMV times out, $\overline{QM}$ returns to High, CNIC is powered down.

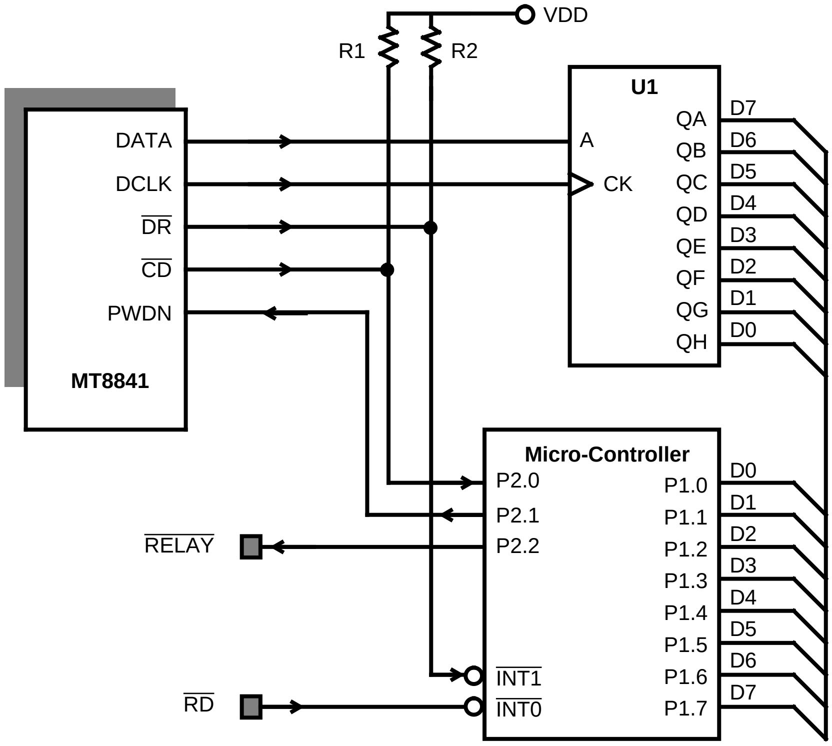
Figure 4 - Logic Controller Timing

Micro-Controller Serial Read

In another interfacing method (not shown here), DATA and DCLK are connected directly to two inputs of a micro-controller port, and $\overline{DR}$ is connected to the interrupt input. This eliminates the serial to parallel shift register but increases the complexity of the software. In this configuration, the micro-controller polls the DCLK bit and stores the DATA value on every DCLK low to high transition. DCLK toggles high eight times for each character. When $\overline{DR}$ pulses low, it marks the end of the 8-bit character (and 10-bit word).

Multiple Line CID Card

Another advantage of the three pin interface is that it is easy to use in applications where multiple CID chips are required on the same card. This card could, for example, be used in a PBX so that a CID device needn't be built into every phone in the building. This would also permit the use of existing display station sets. In such a system, the number of CNIC's could equal the number of incoming lines from the central office. Since the number of incoming lines is much smaller than the number of station lines, the total number of CNIC's required for a system can be greatly reduced. This CNIC card could have many CNIC's with only a single inexpensive micro-controller used to convert the



Components List:

U1	74HC164 Serial-to-Parallel Shift Register
R1,2	10k, 1/2W 1%, Resistor Metal

Notes:

1. Decoupling not shown.
2. U1 powered from +5V.
3. The micro-controller is symbolic and circuitry may vary depending upon micro selected.

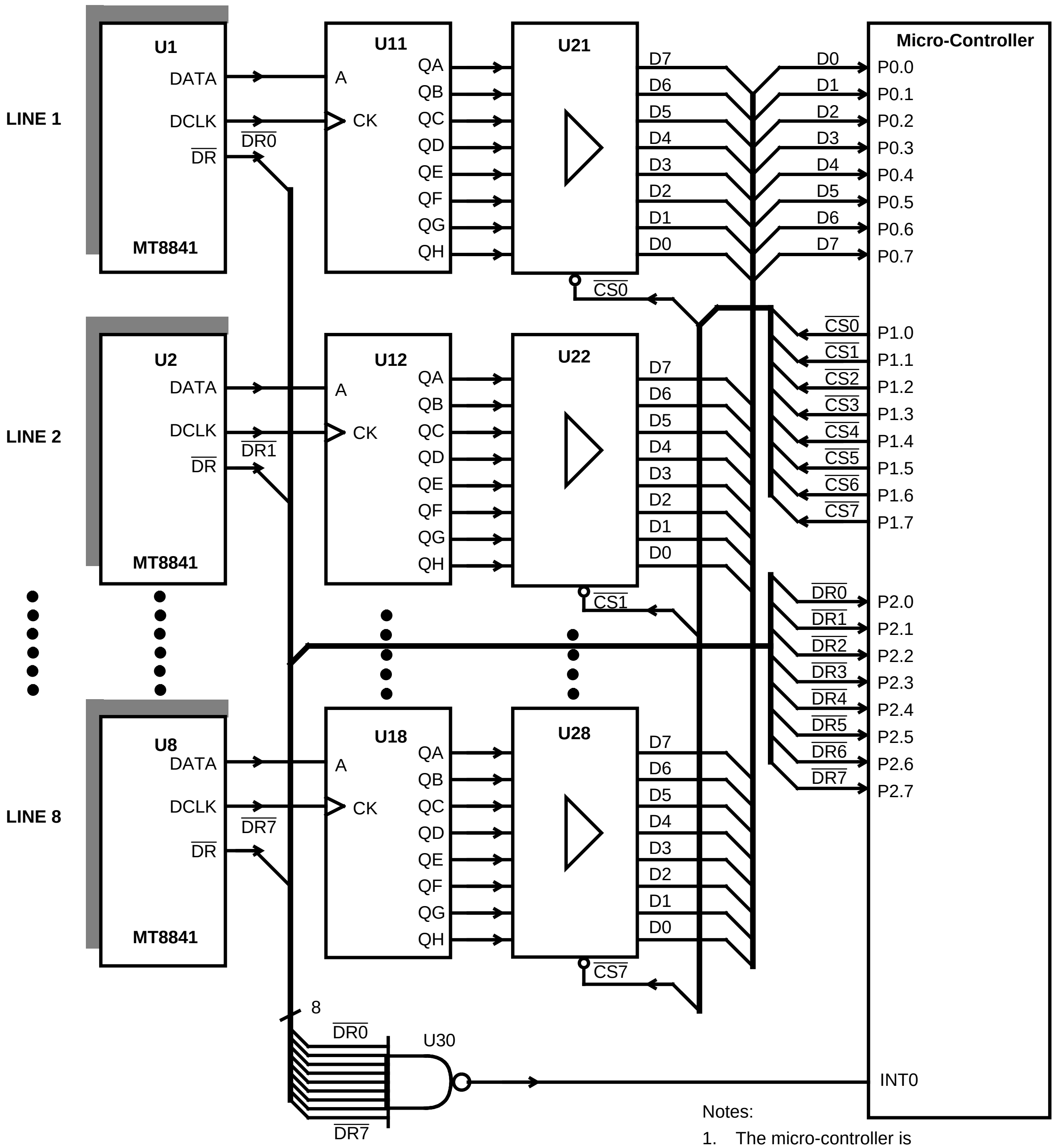
Figure 5 - Micro-Controller and Serial-to-Parallel Converter

code for the caller identification for all of the chips, and no UARTs would be required. The micro-controller would then pass on the data to the receiving station set according to the PBX protocol.

In this CNIC card application, all $\overline{\text{DR}}$ signals are tied into a single interrupt on the micro-controller. Each CNIC DATA and $\overline{\text{DR}}$ output is connected into a serial to parallel shift register with a tri-state output enable. The tri-state outputs are all bussed together and connected to an input port of the micro-controller. All shift register tri-state output enables are driven by an output port. All $\overline{\text{DR}}$ signals are also input to another input port. Upon receiving an interrupt, the micro-controller polls the $\overline{\text{DR}}$ lines to determine which CNIC has delivered data to its shift register. The micro-controller then enables the tri-state output corresponding to the activated $\overline{\text{DR}}$ and reads the 8 bit data at its input port (see Fig. 6)

A Final Word

Caller ID and related technologies will open up many new applications for both telephone companies and their customers. The technology promises to help us gain control over the telephone instead of it controlling us. Best of all, the technology is relatively simple and easily implemented, using the inexpensive devices now available on the market.



Notes:

1. The micro-controller is symbolic and circuitry may vary depending upon micro selected.
2. Port 2.X has pull-up resistors.
3. Decoupling not shown.
4. Power not shown.

Components List:

U1-8	MT8841 CNIC
U11-18	74HC164 Serial-to-Parallel Shift Register
U21-28	74HC241 Octal Tri-State Buffer
U30	74HC30 8 Input Nand Gate

Figure 6 - Multiple Line CID Card

Notes:

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